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09/667,122	09/21/2000	William C. Moyer	SC11306TH	9170

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Austin Intellectual Property Law Section
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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	PAPER NUMBER
2183	2

DATE MAILED: 07/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/667,122	MOYER ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *5,9,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-20 have been examined.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claim 5 is objected to because of the following informalities: The examiner believes that the last word of the claim ("signal") should be changed to --signals--. Appropriate correction is required.

4. Claim 9 is objected to because of the following informalities: Please insert a period at the end of the claim. Appropriate correction is required.

5. Claim 11 is objected to because of the following informalities: The examiner is unclear of the meaning of the limitation "an execution unit which provides the branch condition unit." The examiner is unsure if the wording for this limitation is correct. Appropriate correction is required.

6. Claim 12 is objected to because of the following informalities: Please change "claim11" to --claim 11--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-9 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Samra, U.S. Patent No. 6,275,926, in view of Oh, U.S. Patent No. 5,594,765.

9. Referring to claim 1, Samra has taught a processing system for accessing memory, comprising:

a) an address bus for providing a current address and a previous address to memory. See Fig.1, component 165. Note that it is inherent that this memory bus will comprise an address bus since an address must be applied to memory in order to retrieve or store data within the memory.

b) a data bus for receiving information from memory. See Fig.1, component 165 and again note that it is inherent that this memory bus will comprise a data bus in order to transfer data between the CPU and the memory.

c) Samra has not taught generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address. However, Oh has taught such a signal in a counter system used in conjunction with an SDRAM, which is a type of memory that can be found in Samra's system (see column 4, lines 30-35). A person of ordinary skill in the art would have recognized that Oh's system would allow Samra to incorporate burst transfers between the CPU and memory through use of a single address, thereby reducing activity on the address bus since all subsequent addresses are generated from the original address. This

automatic address generation also results in higher speeds since the CPU does not have to generate a new address for each memory access. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Samra's system with that of Oh in order to allow Samra to take advantage of burst transfers. Regarding the first signal, Oh's system includes a signal "LATCH," which denotes the beginning of a burst cycle. See column 3, lines 38-39 and Fig.7. This signal indicates that the current address (being some address generated during burst mode) may not be sequential to the previous address because the burst mode may be set such that an access is occurring in non-sequential (interleaved) mode.

d) Samra has not taught generating a second sequence signal that when negated indicates that the current address is not sequential to the previous address. However, Oh has taught a second signal "seq_int#," which specifies either sequential or non-sequential (interleaved) burst mode. See column 1, lines 11-18, and column 3, lines 16-21. This signal, when negated will indicate that interleaved (or non-sequential mode) has been selected. In this situation, the current address will be non-sequential with respect to the previous address.

e) Finally, Samra has not explicitly taught generating a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address. However, Samra's system does perform branch prediction as shown in column 3, lines 1-8. As is known in the art of branch prediction, if a branch is predicted not-taken, then the current address (address of the instruction to be executed after the branch) will be sequential to the previous address (since the instruction following the branch, in program order, will be speculatively fetched based on the prediction). However, if it is determined that the branch direction was mispredicted, then a third signal must inherently exist

which indicates that a misprediction has occurred. Such a signal may cause a pipeline flush and the fetching of the appropriate instructions, for instance. For the example where the branch was predicted not-taken, this third signal would indicate that the current instruction address is not sequential to the previous instruction address. Instead, the current address would be the branch target address.

10. Referring to claim 2, Samra in view of Oh has taught a processing system as described in claim 1. Oh has further taught that if the current address is not sequential to the previous address, the first sequence signal is negated prior to the second sequence signal being negated. It should be noted that in order to be in sequential or interleaved burst mode, the system must first be in a general burst mode. Therefore, the first signal (LATCH) will provide an indication before the second signal (seq_int#).

11. Referring to claim 3, Samra has taught a processing system for accessing memory, comprising:

a) an address bus for providing a current address and a previous address to memory. See Fig.1, component 165. Note that it is inherent that this memory bus will comprise an address bus since an address must be applied to memory in order to retrieve or store data within the memory.

b) a data bus for receiving information from memory. See Fig.1, component 165 and again note that it is inherent that this memory bus will comprise a data bus in order to transfer data between the CPU and the memory.

c) an execution unit which generates branch conditions and data addresses. See Fig.2, component 255, and column 5, lines 1-6. Note that the execution unit 255 produces flag results

(conditions based on operations) and also note that data is fetched by the execution unit 255 from the level-1 data cache, which means that it must generate data addresses.

d) a decode control unit which decodes instructions. See Fig.2, component 230.

e) Samra has not taught a fetch unit, coupled to the execution unit, the decode control unit, the address bus, and the data bus, for generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address. However, Oh has taught such a signal in a counter system used in conjunction with an SDRAM, which is a type of memory that can be found in Samra's system (see column 4, lines 30-35). A person of ordinary skill in the art would have recognized that Oh's system would allow Samra to incorporate burst transfers between the CPU and memory through use of a single address, thereby reducing activity on the address bus since all subsequent addresses are generated from the original address. This automatic address generation also results in higher speeds since the CPU does not have to generate a new address for each memory access. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Samra's system with that of Oh in order to allow Samra to take advantage of burst transfers. Regarding the first signal, Oh's system includes a signal "LATCH," which denotes the beginning of a burst cycle. See column 3, lines 38-39 and Fig.7. This signal indicates that the current address (being some address generated during burst mode) may not be sequential to the previous address because the burst mode may be set such that an access is occurring in non-sequential (interleaved) mode.

f) Samra has not taught a unit for generating a second sequence signal that when negated indicates that the current address is not sequential to the previous address. However, Oh has taught a second signal "seq_int#," which specifies either sequential or non-sequential

(interleaved) burst mode. See column 1, lines 11-18, and column 3, lines 16-21. This signal, when negated will indicate that interleaved (or non-sequential mode) has been selected. In this situation, the current address will be non-sequential with respect to the previous address.

g) Samra has not explicitly taught a unit for generating a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address. However, Samra's system does perform branch prediction as shown in column 3, lines 1-8. As is known in the art of branch prediction, if a branch is predicted not-taken, then the current address (address of the instruction to be executed after the branch) will be sequential to the previous address (since the instruction following the branch, in program order, will be speculatively fetched based on the prediction). However, if it is determined that the branch direction was mispredicted, then a third signal must inherently exist which indicates that a misprediction has occurred. Such a signal may cause a pipeline flush and the fetching of the appropriate instructions, for instance. For the example where the branch was predicted not-taken, this third signal would indicate that the current instruction address is not sequential to the previous instruction address. Instead, the current address would be the branch target address.

12. Referring to claim 4, Samra in view of Oh has taught a processing system as described in claim 3. Samra in view of Oh has not explicitly taught that the decode control unit comprises an instruction register. However, Official Notice is taken that an instruction register and its purpose is well known and expected in the art. The instruction register is used to store an instruction which will be decoded into signals used to control the operation of the processor. Consequently,

it would have been obvious to one of ordinary skill in the art at the time of the invention to provide such a component so that a particular instruction can be decoded.

13. Referring to claim 5, Samra in view of Oh has taught a processing system as described in claim 3. Samra in view of Oh has further taught that the fetch unit comprises an address control unit, coupled to the decode control unit (Fig.2, component 230) and the execution unit (Fig.2, component 255), for receiving a branch condition signal from the execution unit (column 5, lines 1-8 and note in Fig.2 that flag results are received) and a branch decode signal and a load/store signal (it is inherent that if a branch is to be executed then a branch decode signal will be provided. Likewise, if a load/store is to be executed, then the appropriate signal should be provided) from the decode unit and for providing the first, second, and third sequence signal. It should be noted by the applicant that the address control unit could be broadly interpreted as comprising the branch unit 270, the load store unit 265, the BTB 275, the fetcher 215 (all components taught by Samra in Fig.2), and the component taught by Oh, allowing for burst transfers. These components all play a part in determining what addresses are applied to memory and therefore, they form a unit which controls addressing. This unit also would be responsible for providing all three of the sequence signals (the first two from Oh's system and the third from the branch's execution).

14. Referring to claim 6, Samra in view of Oh has taught a processing system as described in claim 5. Samra has further taught that the execution unit comprises a condition generator that provides the branch condition signal. See column 5, lines 1-8 and note that the execution unit provides flags (conditions) which are used to determine whether or not a branch is taken.

15. Referring to claim 7, Samra in view of Oh has taught a processing system as described in claim 6. Samra has further taught that the execution unit comprises a data address generator which provides a data address signal to the fetch unit. Note from Fig.2 that data is fetched by the execution unit 255 from the level-1 data cache, which means that it must provide data addresses to the logic that utilizes the generated address in order to fetch from the cache.

16. Referring to claims 8 and 9, Samra in view of Oh has taught a processing system as described in claims 7 and 3, respectively. Oh has further taught that if the current address is not sequential to the previous address, the first sequence signal is negated prior to the second sequence signal being negated. It should be noted that in order to be in sequential or interleaved burst mode, the system must first be in a general burst mode. Therefore, the first signal (LATCH) will provide an indication before the second signal (seq_int#).

17. Referring to claim 13, Samra has taught a processing system comprising:

a) an execution unit. See Fig.2, components 255, 260, 265, and 270.

b) a decode control unit. See Fig.2, component 230.

c) Samra has not taught a fetch unit, coupled to the execution unit and the decode control unit, for providing addresses on an address bus which may be sequential and providing a first sequence signal which indicates if a current address may be sequential to a previous address. However, Oh has taught such a signal in a counter system used in conjunction with an SDRAM, which is a type of memory that can be found in Samra's system (see column 4, lines 30-35). A person of ordinary skill in the art would have recognized that Oh's system would allow Samra to incorporate burst transfers between the CPU and memory through use of a single address, thereby reducing activity on the address bus since all subsequent addresses are generated from

the original address. This automatic address generation also results in higher speeds since the CPU does not have to generate a new address for each memory access. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Samra's system with that of Oh in order to allow Samra to take advantage of burst transfers. Regarding the first signal, Oh's system includes a signal "LATCH," which denotes the beginning of a burst cycle. See column 3, lines 38-39 and Fig.7. This signal indicates that the current address (being some address generated during burst mode) may be sequential to the previous address because the burst mode may be set such that an access is occurring in sequential mode.

d) Samra has not taught a unit for providing a second sequence signal which indicates if the current address is sequential to the previous address. However, Oh has taught a second signal "seq_int#," which specifies either sequential or non-sequential (interleaved) burst mode. See column 1, lines 11-18, and column 3, lines 16-21. This signal, when asserted, will indicate that sequential mode has been selected. In this situation, the current address will be sequential with respect to the previous address.

18. Referring to claim 14, Samra in view of Oh has taught a processing system as described in claim 13. Oh has further taught that if the second sequence signal indicates that the current address is not sequential to the previous address, the first sequence signal indicates that the current address may not be sequential to the previous address prior to the second sequence signal indicating that the current address is not sequential to the previous address.. It should be noted that in order to be in sequential or interleaved burst mode, the system must first be in a general burst mode. Therefore, the first signal (LATCH) will provide an indication before the second signal (seq_int#).

19. Referring to claim 15, Samra in view of Oh has taught a processing system as described in claim 14. Samra has not explicitly taught generating a third sequence signal which indicates if a current instruction address is sequential to a previous instruction address. However, Samra's system does perform branch prediction as shown in column 3, lines 1-8. As is known in the art of branch prediction, if a branch is predicted not-taken, then the current address (address of the instruction to be executed after the branch) will be sequential to the previous address (since the instruction following the branch, in program order, will be speculatively fetched based on the prediction). However, if it is determined that the branch direction was mispredicted, then a third signal must inherently exist which indicates that a misprediction has occurred. Such a signal may cause a pipeline flush and the fetching of the appropriate instructions, for instance. For the example where the branch was predicted not-taken, this third signal would indicate that the current instruction address is not sequential to the previous instruction address. Instead, the current address would be the branch target address.

20. Referring to claim 16, Samra in view of Oh has taught a processing system as described in claim 15. Samra has further taught that the execution unit comprises a condition generator that provides a branch condition signal to the fetch unit. See column 5, lines 1-8 and note that the execution unit 255 provides flags (conditions) which are used to determine whether or not a branch is taken.

21. Referring to claim 17, Samra in view of Oh has taught a processing system as described in claim 16. Samra has further taught that the decode control unit provides a branch decode signal and a load/store signal to the fetch unit. For instance, see Fig.2 and note that the branch unit 270 and load-store unit 265 receive decoded information sent along by the decoder 230.

Furthermore, it is inherent that if a branch is to be executed then a branch decode signal will be provided. Likewise, if a load/store is to be executed, then the appropriate signal should be provided. These signals direct the operation of the appropriate execution units.

22. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christie et al., U.S. patent No. 6,151,662 (herein referred to as Christie), in view of Oh, as applied above.

23. Referring to claim 10, Christie has taught a processing system for fetching instructions and data, comprising:

a) an address bus for providing a current address for retrieving a first instruction, a previous address for retrieving a second instruction, and a data address for retrieving data, wherein the data address occurs before the current address and after the previous address. From Fig.1, it can be seen that the data and instruction caches are both connected to the main memory subsystem, so that if a cache miss occurs, the corresponding instructions and data can be fetched from main memory. It is inherent that this connection (bus) to main memory comprises an address bus so that an address can be applied to main memory. In addition, it should be realized by the applicant that interleaving instruction and data fetches are well known and expected in the art. As instructions are fetched and executed, the need to fetch data also exists for operands (for instructions such as Add, or Subtract) and from memory addresses (for loads). Therefore, fetching data can occur between the fetching of two instructions.

b) a data bus for retrieving the first and second instructions and the data. Again, it can be seen from Fig.1 that the data and instruction caches are both connected to the main memory subsystem, so that if a cache miss occurs, the corresponding instructions and data can be fetched

from main memory. It is inherent that this memory bus will comprise a data bus in order to transfer data between the CPU's caches and the memory.

c) Christie has not explicitly taught a fetch unit, coupled to the address bus and the data bus, for generating a first sequence signal that when asserted for the current address indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address. However, Oh has taught such a signal in a counter system used in conjunction with an SDRAM, which is a type of memory that can be found in Christie's system (see column 13, lines 29-33). A person of ordinary skill in the art would have recognized that Oh's system would allow Christie to incorporate burst transfers between the CPU and memory through use of a single address, thereby reducing activity on the address bus since all subsequent addresses are generated from the original address. This automatic address generation also results in higher speeds since the CPU does not have to generate a new address for each memory access. As a result it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Christie's system with that of Oh in order to allow Christie to take advantage of burst transfers. Regarding the claimed signal, Oh's system includes a signal "seq_int#" which, when asserted (sequential mode), indicates that the current address is sequential to the previous address. On the other hand, when negated, the "seq_int#" signal indicates that the current address may not sequential to the previous address (interleaved mode). See column 1, lines 11-18, and column 3, lines 18-23.

24. Referring to claim 11, Christie in view of Oh has taught a processing system as described in claim 10. Christie in view of Oh has further taught that the fetch unit comprises an address control unit for receiving a branch condition, a branch decode signal, and a load/store signal and

for providing the first sequence signal. It should be noted by the applicant that the address control unit could be broadly interpreted as comprising an execution unit 18 for executing a branch, a load-store unit 20 (taught by Christie in Fig.1), and the component taught by Oh, allowing for burst transfers. These components all play a part in determining what addresses are applied to memory and therefore, they form a unit which controls addressing. In addition, the branch execution unit would inherently receive a branch condition so that it knows whether to execute the branch or not and it would also inherently receive a branch decode signal so that the execution unit knows that it is executing a branch instruction (this can also be seen in Fig.2, where the decoder provides signals to the reservation stations, which are then subsequently provided to the execution units). Furthermore, the load-store unit 20 would receive a load-store signal (for instance, signals 80, 82, and 84 shown in Fig.4). This unit also would be responsible for providing the first sequence signals (since Oh's system provides such a signal, and this system can be considered part of the address control unit).

25. Referring to claim 12, Christie in view of Oh has taught a processing system as described in claim 11. Christie has further taught:

a) an execution unit which provides the branch condition unit. It is inherent that if a system includes conditional branches, then conditions must be provided. These conditions are set based on a result achieved from performing an arithmetic operation.

b) a decode control unit which provides the branch decode signal and the load/store signal. See Fig.1, component 16. It should be realized that a branch execution unit 18 would inherently receive a branch decode signal so that the execution unit knows that it is executing a branch instruction (this can also be seen in Fig.2, where the decoder provides signals to the reservation

stations, which are then subsequently provided to the execution units). Furthermore, the load-store unit 20 would receive a load-store signal from the decoder via reservation station (for instance, signals 80, 82, and 84 shown in Fig.4).

26. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christie, as applied above.

27. Referring to claim 18, Christie has taught a processing unit comprising:

a) an execution unit. See Fig.1, components 18.

b) a decode control unit. See Fig.1, component 16.

c) Christie has not explicitly taught a fetch unit, coupled to the execution unit and the decode unit, for providing instruction and data addresses on an address bus and providing a first sequence signal that indicates if a current instruction address is sequential to a previous instruction address even if a data address is provided between the current instruction address and the previous instruction address. However, Christie's system does perform branch prediction as shown in column 6, lines 59-61, and column 8, lines 5-10. As is known in the art of branch prediction, if a branch is predicted not-taken, then the current address (address of the instruction to be executed after the branch) will be sequential to the previous address (since the instruction following the branch, in program order, will be speculatively fetched based on the prediction). However, if it is determined that the branch direction was mispredicted, then a third signal must inherently exist which indicates that a misprediction has occurred. Such a signal may cause a pipeline flush and the fetching of the appropriate instructions, for instance. For the example where the branch was predicted not-taken, this third signal would indicate that the current

instruction address is not sequential to the previous instruction address. Instead, the current address would be the branch target address. Therefore, in order to achieve misprediction recovery, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a signal that specifies whether or not a current instruction address is sequential to a previous instruction address even if a data address is provided between the current instruction address and the previous instruction address.

28. Referring to claim 19, Christie has taught a processing unit as described in claim 18. Furthermore, it is inherent that if a system includes conditional branches, then conditions must be provided by some execution unit. These conditions are set based on a result achieved from performing an arithmetic operation within an execution unit. For instance, if the result of some addition operation is zero, then a flag indicating zero would be set so that any conditional branches that check for a zero result, will be able to utilize the flag (condition).

29. Referring to claim 20, Christie has taught a processing unit as described in claim 19. Christie has further taught that the decode control unit provides a branch decode signal and a load/store signal to the fetch unit. See Fig.1, component 16. It should be realized that a branch execution unit 18 would inherently receive a branch decode signal so that the execution unit knows that it is executing a branch instruction (this can also be seen in Fig.2, where the decoder provides signals to the reservation stations, which are then subsequently provided to the execution units). Furthermore, the load-store unit 20 would receive a load-store signal from the decoder via reservation station (for instance, signals 80, 82, and 84 shown in Fig.4).

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Inagaki et al., U.S. Patent No. 5,835,969, has taught an address test pattern generator for burst transfer operation of an SDRAM. Multiple signals are used which implicitly specify whether a current address will be sequential to the previous address.

Thome et al., U.S. Patent No. 5,809,549, has taught burst SRAMs for use with a high speed clock.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
July 21, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100